

Josephson Computer Technology: An IBM Research Project

This special issue of the IBM Journal of Research and Development describes the status of IBM's research project on Josephson computer technology. This first paper traces the origins and history of Josephson technology as it led to the project and outlines the project's scope. The potential of the technology for ultrahigh-performance computer mainframes is discussed and the major technological characteristics of LSI Josephson devices are examined. The paper then provides an overview outline of the remaining papers presented in this issue.

Technology and project origins

This issue is devoted entirely to IBM's Josephson Computer Technology Project, which is currently being pursued by IBM Research in Yorktown, Zurich, and East Fishkill and is aimed at demonstration of system and technological feasibility of Josephson devices for computer application. Josephson LSI digital circuits have the potential for outperforming Si and GaAs semiconductor LSI circuits in both circuit speed and overall system performance. Such devices have in fact excellent potential for the realization of reliable computer mainframes with ultrahigh performance.

Josephson devices are based on superconductivity, tunneling, and the Josephson effects; they must therefore be operated at very low temperatures of about 4° above the absolute zero temperature (of -273.16°C). Superconductivity manifests itself as zero electrical resistance, which was discovered by Kammerlingh Onnes [1] in 1911, and by its almost perfect diamagnetic behavior as first observed by Meissner and Ochsenfeld [2] in 1933.

Superconductors were first proposed for digital circuits by D. Buck [3] in 1956 when he reported that cryotrons—as he named these switching devices—could be switched from a superconducting to a normal conducting state by application of magnetic fields which quenched superconductivity in samples held just below their transition temperature. His ideas were picked up in several laboratories and explored on a broad basis until it was discov-

ered that switching speed was severely limited and not competitive with then emerging integrated transistor circuits.

From its initial discovery in 1911 it took almost 50 years for the origin and properties of superconductivity to be satisfactorily explained by Bardeen, Cooper, and Schrieffer [4] in 1957 in their now famous BCS theory of superconductivity. This theory postulates that certain electrons condense into a paired state when superconductors are cooled, and that these electron pairs (or Cooper pairs) are responsible for all superconducting properties, among them the so-called superconducting energy gap which acts similarly to a forbidden energy band in semiconductors. The existence of this energy gap was demonstrated in 1960 by Giaever [5], who used a superconducting tunneling structure and demonstrated that electrons cannot tunnel when the superconducting energy gaps of both superconductors across the tunnel barrier are not properly aligned.

On the basis of equations of the BCS theory, Josephson [6] predicted in 1962 that interactions of electrical potential and magnetic fields with the Cooper pair system should be observable in so-called weakly coupled superconducting regions, of which a Giaever-type superconducting tunneling structure is an example. Josephson's prediction of dc-Josephson current—as it is now known—and its dependence on magnetic flux were exper-

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imentally verified at Bell Telephone Laboratories [7] in 1963, and work was begun in 1964 at IBM Research to study the potentially fast switching speed of thin-film Josephson devices for digital circuit applications. This work culminated in 1966 in demonstration of subnanosecond switching of Josephson tunneling devices [8], and in 1967 in the operation of a thin-film Josephson device flip-flop [9], both indicating that Josephson switching devices could indeed be switched very fast and could be competitive with projected semiconductor integrated circuits. On the basis of these encouraging results, the pros and cons of Josephson devices were assessed [10] and an initially small research program was launched in 1967 with the aim of studying technological and system aspects.

The project reported on in this issue has been in existence ever since; it has grown in scope and has achieved several milestone accomplishments, including an invention for reproducible tunnel barrier formation [11], material and process selections for devices which sustain many cool-down and warm-up cycles [12], devices and circuits with very short switching and logic delays [13, 14] and, more recently, the demonstration of LSI-type circuit chips and of components [15-18] and of a novel package concept [19] commensurate with ultrahigh-performance operation.

The scope of the present program ranges from materials and process studies to device modeling and to logic and memory circuit design, fabrication and testing; it encompasses exploration of novel packaging, design automation, and testing concepts commensurate with high-speed LSI technology. The program's current status is the subject of this special issue; this initial paper presents a perspective of the system potential and the technical characteristics of Josephson computer technology.

System aspects

Josephson computer technology provides excellent potential for ultrahigh-performance computer mainframes complete with processors and memory hierarchies. Ultrahigh performance may be defined in this context as ranging from 500 to 5000 ps in processor cycle time with commensurately fast-access cache and main memories to support such ultrahigh-performance processors. This range of processor cycle times, combined with current computer architecture, could provide mainframes with 10- to 100-fold higher computing rates than that of an IBM 3033 mainframe system.

It is illustrative to assess the implications of ultrahigh performance as defined above by postulating a hypothetical mainframe, without regard to technology, comprising a 1-ns uniprocessor backed by a 2-ns cache and a 10-ns

main memory. If constructed in IBM 3033 system architecture, it is estimated that this mainframe would provide about 250 MIPS (millions of instructions per second) of computing power and it would comprise about 300 000 processor circuits, 256K bytes of cache and at least 64M bytes of main memory capacities [20], the latter increased about eight to ten fold over current main memory capacities in an attempt to bridge the access gap between the contemplated ultrahigh-performance mainframe and conventional I/O and auxiliary storage systems.

One may subdivide the time span of the postulated 1-ns processor cycle into 400 ps for on-chip logic delay which, for an average of ten serially connected logic stages, mandates a logic family with 40 ps logic delay per stage; one may allot 500 ps to off-chip delays incurred in signal lines which interconnect chips and one finds consequently that the total interchip wiring length of a worst-case logic path in a processor subnetwork must not exceed 8 cm; this would then leave 100 ps to allow for timing margins.

Similarly, the total postulated access times of 2 and 10 ns for cache and main memory, respectively, may be subdivided as follows. One may allot 600 ps for on-chip cache access and 1400 ps for transmitting an address from the processor to the cache chips and data back from the cache chips to the processor, which means that the signal path length between them must not exceed 11 cm. One may further allot 7 ns for on-chip main memory access, leaving 3 ns for package delay throughout the total main memory. The propagation time of 3 ns demands that overall main memory linear dimensions be kept below 30 cm. Today's experimental Josephson logic and memory circuits do not quite measure up to the required values, yet they are estimated to approach them already to within a factor of about two.

Such a mainframe needs to be packaged into a volume of less than $10 \times 8 \times 8$ cm—its processor into $6 \times 4 \times 4$ cm—in order to conform to the maximum linear dimensions previously cited, with lines being routed in rectangular fashion. A problem in doing that with current and projected semiconductor LSI circuits of sufficiently high performance arises because of the high levels of power dissipated on chips during circuit operation. If the hypothetical mainframe were implemented with semiconductor technology as used in the IBM 3033 system, it would dissipate (even with only 8M bytes of main memory) about 20 kW of power, an amount impossible to extract from such a small volume with today's cooling technology.

Future miniaturization of semiconductor circuits is likely to reduce power dissipation per circuit, yet even a

tenfold decrease would still make it difficult, if not impossible, to extract that heat from the exceedingly small volume while keeping circuits at proper operating temperature. Immersion in a cryogenic liquid such as liquid nitrogen would not alleviate the problem either because of the onset of film boiling, to be discussed in the next section, which leads to thermal runaway and superheating of chips by several hundred degrees.

The hypothetical ultrahigh-performance mainframe is, in contrast, estimated to dissipate less than 10 W when constructed with future Josephson circuit chips (with somewhat higher density than those described in this issue). This amount of heat could readily be extracted from the volume of $10 \times 8 \times 8$ cm by immersion of the packaged mainframe in a liquid helium bath. It appears, therefore, that Josephson technology may, at present, be the only one with potential for construction of mainframes of the ultrahigh performance defined previously.

A more detailed treatment of the implementation of a mainframe system with about 70 MIPS performance, based on circuit and package approaches under experimental investigation to date, is given elsewhere [21]. That publication also deals with refrigeration and input-output aspects across the cryogenic-room temperature interface.

The need for Josephson technology mainframes to be kept at near zero absolute temperatures for operation is conveniently satisfied by immersing them in a liquid helium bath which boils off as the internal power dissipation of the mainframe imparts heat to it. The heat influx through cryostat walls and I/O signal lines which connect the mainframe with semiconductor interface circuits at room temperature will cause additional boiling. The helium vapor is compressed at room temperature and resupplied to a liquid helium refrigerator for closed cycle operation. The refrigerator is housed with the computer mainframe in the same cryostat, the compressor is a stand-alone unit. The total electrical input power to drive the compressor is, for thermodynamic and efficiency reasons, about 2000 times greater than the cooling power of the refrigerator. Refrigeration of the hypothetical mainframe would therefore require 20 kW of unregulated ac power.

The need for the low-temperature environment causes additional refrigerator cost and inconvenience for system debug and servicing; yet it provides significant benefits which will be discussed in the next section, among them a potential for high reliability and longevity of components. This aspect may allow assembly of much larger multiprocessor mainframes than is practical to date with unprecedented performance and storage capability.

Cost overhead for refrigeration may not be much of a disadvantage, at least for large- and medium-scale mainframes. This becomes clear if one compares combined power supply and cooling equipment cost for semiconductor and Josephson technology systems. With current semiconductor technology the combined equipment cost for power supply and cooling will likely exceed that for projected Josephson mainframes by a relatively wide margin, and it is expected that for future semiconductor mainframes (with reduced power supply cost) the combined cost will still remain at least as high as for Josephson technology mainframes with equivalent circuit count yet substantially improved performance.

Also, Josephson chip and circuit cost is expected to be similar to semiconductor technology for the same lithographic resolution since process cost, yield and circuit density can be asserted to be similar. Consequently, total costs for mainframes with equal circuit count and including power supply and cooling are likely to remain similar for both technologies, which gives Josephson technology a cost/performance advantage, in terms of cost per executed instruction, since the Josephson mainframe can execute many more instructions per second.

Ultrahigh-performance systems are not the only viable application for Josephson computer technology. It is quite conceivable that fast switching speed can be used to lower logic circuit count, leading to implementation of mainframes with fewer chips of faster circuits. Thus, design, fabrication, and testing cost may be reduced. This trend would seem to be counteracted by the relatively fixed cost of commercially available liquid helium refrigerators; yet the exploration of microcoolers [22], which has just recently begun, opens new avenues for competitiveness in this respect. Microcoolers may conceivably be constructed with microcircuit processing methods. If and when they become a reality, they may allow the assembly of minicomputers or other small-size special-purpose computers, perhaps with A to D converters and magnetometers or microwave instruments, all based on Josephson devices, and with microcoolers of very small dimensions and small thermal mass. Such systems may conceivably be cooled on demand, requiring electrical power only during their operation. They could provide electronic instrumentation with unprecedented sensitivity and accuracy.

Technology characteristics

Josephson devices are attractive for ultrahigh-performance computers because of the combination of three characteristics: (a) extremely fast switching (<10 ps), (b) extremely low power dissipation (<500 nW per circuit), and (c) operation at very low temperatures (≈ 4 K).

The first characteristic is clearly a prerequisite for fast logic speed and cache memory access. It poses, however, problems which will be common to all technologies attempting to reach into the ultrahigh-performance range as defined in the previous section. These problems arise since electrical signal pulses with rise times of less than 10 ps render all strip lines of more than about 2-mm length on-chip and throughout a package electrically long. It is therefore advisable to terminate these lines properly and it is mandatory to match discontinuities along their lengths, *e.g.*, fan-out tabs, beam leads, solder bonds, and pluggable connectors, to the line impedance. This avoids signal reflections and distortion, and thus reduces effective signal delay and disturbance. Such signals, with frequency spectra up to 35 GHz, will also substantially couple into adjacent and crossing lines unless proper precautions are taken, as anyone familiar with microwave technology will appreciate. How one might solve these problems in room-temperature semiconductor technologies is not clear to date, yet it appears that solutions are at hand in Josephson technology, as a subsequent discussion will show.

The second characteristic, low power dissipation, offers advantages since it allows the transfer of heat directly from chips into the liquid coolant bath. This is in contrast with the need for voluminous heat sinks necessary in current high-performance semiconductor technology to prevent thermal runaway. Circuit miniaturization will not alleviate this problem in semiconductor technology, since the density of circuits is likely to go up faster than the power per circuit decreases, thus causing the chip power density to remain high, especially if higher switching speed is demanded. Cooling in liquid nitrogen will not alleviate this problem either because chips would be superheated by several hundreds of degrees at the onset of film boiling once the "critical power density" was exceeded. Since the power dissipation of Josephson logic and cache memory chips, for current experimental circuits, is more than three orders of magnitude smaller, they will not suffer from this problem.

Low power dissipation also permits resistive termination of all strip lines on-chip and throughout the package. In fact the power dissipation of 500 nW per circuit previously cited includes the power dissipated in the line termination resistors, and it is planned to terminate all signal lines in Josephson processors and to do it on-chip. Direct heat transfer from chip to bath is not impeded by this measure.

Furthermore, low power dissipation avoids an increasingly difficult problem observed in high-performance semiconductor technologies as they are miniaturized.

This is the problem of disturbs on power busses caused by logic circuits consuming different amounts of power in their *on* and *off* states, which causes the nominal power supply voltage or current to change when the circuits switch. The disturb must be transmitted to the nearest power regulator and the nominal voltage or current levels must be restored and transmitted back to the logic circuit before it can regain its nominal operating point. A distance of only 1.5 cm between circuit and power regulator renders the circuit off its nominal operating point for as long as 200 ps under ideal transmission characteristics along the voltage or current bus, and longer in practice. This problem is eliminated in Josephson technology by arranging voltage regulators on-chip such that no logic circuit is further than about 40 ps away from its nearest regulator, and by providing current limiting resistors to each logic circuit. These measures increase the total power to be supplied to a chip about ten fold over the actual power requirement of its circuits, yet direct heat transfer is not impeded.

The third characteristic, low operating temperature, not commonly recognized as a benefit, can provide very desirable features for ultrahigh-performance computers, since the low temperature allows the use of superconducting strip lines and ground planes with zero electrical resistance. The strip lines can therefore transmit electrical signals unattenuated and with minimum distortion (when properly terminated) even when they are arranged close to the ground plane, made thin and narrow, and are closely spaced. Close proximity to a ground plane yields low characteristic impedance and all but eliminates crosstalk between parallel and crossing lines. Thin lines provide a low aspect ratio of height to width which is beneficial for microcircuit fabrication and lithographic patterning. Narrow and closely spaced lines provide high wiring-channel density and thus are favorable for system wiring. It is estimated that one *x*- and one *y*-wiring plane will suffice on-chip and throughout the package for total interchip connections in Josephson mainframes.

Low temperature can provide still more benefits. The thermal energy (kT) is about 100 times smaller at 4 K than at 360 to 380 K where semiconductor circuits are operated. This leads to smaller thermally induced electrical noise, and helps to maintain good signal-to-noise ratio even when signal bandwidth is increased and signal energy is reduced. The low energy (kT) also affects the rates of thermally activated physical and chemical processes such as diffusion, corrosion, and electromigration. These processes are temperature dependent and are at a virtual standstill at 4 K. A potential exists therefore for ultrahigh reliability and longevity of components in Josephson technology.

However, low temperature also introduces specific problems in Josephson technology which are predominantly caused by differential thermal expansion of different materials used on-chip and in the package. In order to minimize this problem one needs to match the thermal expansion coefficient of chip substrates and package components, for example, by using Si wafers for both. The problem persists, nevertheless, since chip substrates, metal, and insulating thin films exhibit dissimilar thermal expansion coefficients. Permanent stress is unavoidably introduced when chips and package are fabricated and assembled at room temperature and operated at 4 K, and transitory stresses may be set up during warm-up and cool-down when temperature gradients develop between different parts. The solution to these problems is a careful selection of materials and processing methods to strengthen materials and structures so that deformations will remain in their elastic range.

Josephson LSI circuit chips, although quite different in their principle of operation, are fabricated similarly to semiconductor LSI chips. Patterning by photo, electron-beam, and x-ray lithography can be used. Metal and insulator film deposition is accomplished by vapor deposition and/or sputtering. The crucial fabrication step is that of tunnel barrier formation, with only 4 nm thickness and requiring extreme thickness control. It is accomplished by an rf sputtering process in a low-pressure oxygen atmosphere. The uniformity and yield of this process appear to be quite adequate for LSI-type logic and memory circuits. Therefore chip cost is likely to be comparable with that of semiconductors, since equipment and complexity of fabrication are expected to be similar.

Contents of this special issue

The remainder of this special issue presents a report on the various aspects of IBM's Josephson computer technology program and its current status.

The paper by Matisoo (overview, logic and memory) discusses the physics underlying the operation of Josephson devices and provides an overview of the electronics aspects of LSI logic and memory, including power supply and clocking schemes. Matisoo's overview is followed by a group of three papers—by Gheewala (current injection logic circuits); by Faris, Henkels, Valsamakias, and Zappe (cache memory); and by Guéret, Moser, and Wolf (main memory). These papers deal with detailed design, analysis, and performance issues of LSI logic, and with non-destructive and destructive read out memories, respectively.

The paper by Brown (overview, Josephson packaging) reviews a package concept and outlines the status of ex-

perimentation with package parts and technology; while the paper by Jones and Herrell (chip-to-chip signal propagation) deals with the electrical characteristics of the first package level, i.e., chip and card, as determined by modeling and experimentation.

Following this, the paper by Broom, Kotyczka, and Moser (Josephson junctions) describes several models for calculating the Josephson current in tunnel junctions of various geometries.

The next paper, by Ames (overview, materials and processes), introduces microcircuit processing and materials aspects related to the fabrication of Josephson circuit chips and wafers. This overview is followed by a group of five related papers, by Greiner *et al.* (fabrication process); Broom, Jaggi, Mohr, and Oosenbrug (process variables, lead-alloy junctions); Broom, Laibowitz, Mohr, and Walter (niobium junctions); Baker, Kircher, and Matthews (tunnel barrier oxides); and Kircher and Lahiri (properties of AuIn₂ resistor films). These papers deal in succession with selected items in the technology area such as, respectively: fabrication processes for LSI circuits based on lead-alloy superconductors, the effect of process variables on electrical properties of tunnel junctions, fabrication and properties of niobium tunnel junctions, structure of tunnel barrier oxides for lead-alloy junctions, and properties of integrated thin-film resistors.

The last paper, by Tsui (Josephson signal processor), outlines the mapping of a small semiconductor signal processor into LSI Josephson technology, and describes its architectural and design features.

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